PATENT ABSTRACTS OF JAPAN

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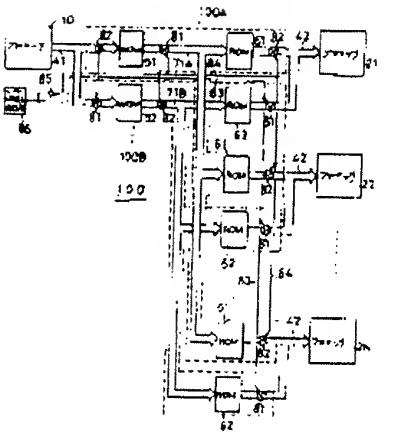
(54) SHARED MEMORY

(57)Abstract:

PURPOSE: To eliminate interruption of processors at the time of data transfer between processors by providing plural write-only memories in the input port of a public memory and plural read-only memories in the output port.

CONSTITUTION: Write-only memories 51, 52 that write data from a processor 10 are provided in the input port of a shared memory 100, and read-only memories 61, 62 that read data to processors 21W2N are provided in output ports. Gates 81, 82 that determine transfer mode of data are provided in an A port 100A and a B port 100B. The gate 81 is connected to a change-over signal generating circuit 86, and the gate 82 is connected to a mode changing signal generating circuit 86 through a controlling line 84 and an invertor 85 for inverting signals. By this way, transfer mode of the A port 100A and B port 100B become reverse.



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